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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,212	10/13/2004	Steven T Peake	GB 020048	2126

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,212	PEAKE, STEVEN T	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 9/30/05 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The application file does not contain a copy of EP 1 033 759 A1.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 thru 9, and 11 thru 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish et al. 5,688,725 in view of Kocon et al. 6,351,009 B1. Darwish discloses (see, for example, FIG. 11G) a vertical trench MOSFET (vertical power transistor trench-gate semiconductor device) comprising a semiconductor body, active area, plurality of electrically parallel transistor cells, gates (trench- gates) 102, N+ source regions (source regions) 112, N-drift region (drain regions) 111, P body (channel-accommodating region) 116, and deep P+ region (ruggedness regions) 114. Darwish does not disclose source regions and the ruggedness regions ... as alternating stripe areas having a width perpendicular to and fully between each of

two adjacent parallel stripe trench-gates. However, Kocon discloses (see, for example, FIG. 3C) trench gates 307 alternating in between P+ body regions 302, and N+ source regions 306. In column 5, lines 1-5, Kocon discloses that such an arrangement exploits the advantage of device size reduction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have source regions and the ruggedness regions ... as alternating stripe areas having a width perpendicular to and fully between each of two adjacent parallel stripe trench-gates in order to exploit the advantage of device size reduction.

Regarding claim 2, Darwish in view of Kocon does not disclose the cell pitch being less than 2 um, and wherein the length of the source region stripes being in the range 10 um to 50 um. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the cell pitch and length of source region stripes in order to have an array of cells adequately operating in a reduced space. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the cell pitch being less than 2 um, and wherein the length of the source region stripes being in the range 10 um to 50 um because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the cell pitch and length of source region stripes in order to have an array of cells adequately operating in a reduced space. See In re Aller, 105 USPQ 233.

Regarding claims 3-9, the limitations contained in claims 3-9 are functions of the cell pitch, and optimized in the same manner as the paragraph above.

Regarding claims 11, and 12, Darwish in view of Kocon does not disclose the doping concentration of the ruggedness regions being approximately 10 times greater than the doping concentration of the source regions, and the doping concentration of the ruggedness regions

being about 10^{21} cm^{-3} and the doping concentration of the source regions being about 10^{20} cm^{-3}. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the doping concentrations of the ruggedness regions and the source regions in order to provide a semiconductor region that can adequately conduct a current from the source to the drain in a vertical trench MOSFET. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the doping concentration of the ruggedness regions being approximately 10 times greater than the doping concentration of the source regions, and the doping concentration of the ruggedness regions being about 10^{21} cm^{-3} and the doping concentration of the source regions being about 10^{20} cm^{-3} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the doping concentrations of the ruggedness regions and the source regions in order to form a semiconductor regions that can adequately conduct a current from the source to the drain. See In re Aller, 105 USPQ 233.

Regarding claim 13, see, for example, FIG. 11G wherein Darwish discloses the deep P+ region extending further into the drift region 111 than the gates 102.

Regarding claim 14, see, for example, column 2, lines 32-36 wherein Darwish discloses the breakdown voltage being likely 60 volts or less (drain-source breakdown voltage of the device is in the range up to about 50 volts).

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Darwish et al. '725 in view of Kocon et al. '009 B1 as applied to claims 1-9, and 11-14 above, and further in view of Mo 6,316,806 B1. Darwish in view of Kocon does not disclose the semiconductor body

being silicon. However, Mo discloses (see, for example, column 3, lines 40-44) a semiconductor device comprising a silicon wafer 44 wherein a trench is formed therein. It would have been obvious to one of ordinary skill in the art at the time of invention to have the semiconductor body being silicon in order to adequately form semiconductor regions in a semiconductor device such as a MOSFET.

Regarding the limitation "the ruggedness regions have ... doping concentration in the range of $10^{10}cm^{-3}$ to 10^{22} cm^{-3}, and wherein the source regions have ... a doping concentration in the range of 10^{18} cm^{-3} to 10^{21} cm^{-3}. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the doping concentrations of the ruggedness regions and the source regions in order to provide a semiconductor region that can adequately conduct a current from the source to the drain in a vertical trench MOSFET. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the ruggedness regions have ... doping concentration in the range of $10^{10}cm^{-3}$ to 10^{22} cm^{-3}, and wherein the source regions have ... a doping concentration in the range of 10^{18} cm^{-3} to 10^{21} cm^{-3} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the doping concentrations of the ruggedness regions and the source regions in order to form a semiconductor regions that can adequately conduct a current from the source to the drain. See In re Aller, 105 USPQ 233.

Response to Arguments

5. Applicant's arguments filed 11/2/05 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 6, lines 1-8 that Darwish does not disclose "ruggedness regions are ... more heavily doped than the channel-accomodating region ... and extend into the drain" and that Office admits that Darwish does not disclose or suggest this feature, this argument is not persuasive. The Office does not admit that Darwish does not disclose this feature. In the Office action filed 8/10/05, the Examiner cited Darwish (see, for example, FIG. 11G) having a P body (channel-accomodating region) 116, and a deep P+ region (ruggedness regions) 114. The deep P+ region is more heavily doped than the P body. Kocon is only used to show the obviousness of having source regions and the ruggedness region ... as alternating stripe areas having a width perpendicular to and fully between each of two adjacent parallel stripe trench-gates, and not the relative doping concentrations, which is already shown in Darwish.

Regarding the applicant's argument on page 7 that the Office needs to establish an artisan in the art is motivated to "optimize" the performance of "[a] vertical power transistor trench-gate semiconductor device" in the exact manner as disclosed in the claimed invention by the above-identified feature of claim 11, this argument is not persuasive. The fact that the applicant uses the MOSFET for a different purpose does not alter the conclusion that its use in prior art device would be prima facie obvious from the purpose disclosed in the reference." In re Lintner, 173 USPQ 560.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
January 7, 2006